

Preamble

Naturally occurring signals are analog; at least at a macroscopic level. The electrical version of natural signals may be prohibitively small for direct digitization for digital signal processing. Also these signals are corrupted by noise and interference. The processing of such signals demands that the front end of receivers be capable of rejecting out-of-band noise and amplifying weak signals with the addition of as little noise as possible. Also most device and circuit parameters vary with the fabrication process, supply voltage and temperature. It is necessary to design analog circuits that remain robust over a range of parameter values. This is a challenging task and it is this set of challenges that shall be addressed in this course.

CMOS technology has come to dominate the analog market as it does the digital domain. The speed of the basic MOS transistor has increased by more than 3 orders of magnitude over the last 3 decades. The scaling of MOS transistors in the analog domain is quite different from that in the digital world – it is more involved. Also lack of device models that accounts for noise and impedance at very high frequencies is a problem quite unique to analog design.

Course Content

- * Basic analog building blocks
- * Opamp design
- * Oscillators and Phase locked loop
- * Scaling for mixed signal applications
- * Data converter fundamentals
- * Sigma-Delta data converters
- * Lab sessions

Speakers

Eminent persons from IITs, Analog Devices, Cosmic Circuits and NIT-Calicut

Eligibility

The course is open to teachers from AICTE approved Engineering Colleges/Polytechnics with a basic qualification in electronics.

Registration Fee

For teachers from AICTE approved institutions / colleges / polytechnics: Rs. 300/- (refundable only if not selected or the course is attended fully on selection). The registration fee shall be paid through a crossed demand draft, drawn in favour of “Co-ordinator, STTPNE” payable at State Bank of India, REC Chathamangalam Branch (Code 2207).

Travel

Participants will be reimbursed travel expenses limited to sleeper class train fare by the shortest route.

How to Apply

Application in the attached form or in a similar format along with the DD for the registration amount and a self-addressed envelope should reach the co-ordinator by 28th April 2009. Application forms can be downloaded from the institute website (www.nitc.ac.in/nitc/sdp/aicte_sdp.htm). Selection shall be on a **first come first served basis** subject to NITC norms.

You shall be intimated about your participation status through e-mail by May 1, 2009.

Address for Correspondence

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